Amendments to the Specification:

Please replace the paragraph starting with "Fig. 4" beginning on page 13, lines 6-11, with the following amended paragraph:

Fig. 4 shows a second embodiment of the clock regenerator unit 1. In this case the configuration and operation of the PLL circuit 4A are described ~~as described~~ with respect to Figure 3 for digital signals traveling from the client equipment to the wavelength division-multiplexing apparatus. The PLL circuit 4B also has a similar configuration for digital signals traveling from the wavelength division-multiplexing apparatus to the client equipment.

Please replace the paragraph starting with "The feedback" beginning on page 13, lines 13-27, with the following amended paragraph:

The feedback loop having a VCO 41, a first frequency divider ~~43~~42, and a phase/frequency comparator 43 operates in a manner similar to that in the first embodiment. In this embodiment, a third oscillator 8 is used in place of the first and second oscillators 7-1 and 7-2 of the first embodiment. The output clock signals from the first frequency divider 42 are inputted into a third frequency divider 51, where the output clock signals are further divided by a specified division ratio. The output clock signals from the third frequency divider 51 are inputted into a rise edge detector circuit 52. A clock counter 53 is reset when the output clock signals from the third frequency divider 51 rise. The clock counter 53 counts the input clock signals from a pin CK, and each time it is reset, the clock counter outputs the preceding count to a register 54. The pin CK for the clock counter 53 contains via input fundamental clock signals for a reference clock count that are generated by the oscillator 8. Therefore, the register 54 stores fundamental clock count values with different values based on the clock cycles that are outputted from the third frequency divider 51. The stored values in the register 54 are inputted into a frequency comparator 55.

Please replace the paragraph starting with "According" beginning on page 15, lines 14-20, with the following amended paragraph:

According to the configuration of the above described second embodiment, a plurality of types of reference clock signals, corresponding to the signal transmission modes, are generated by using one oscillator 8 that generates fundamental clock signals. In addition, the instantaneous comparison of the output clock frequency from the PLL with multiple types of reference clock frequencies permits the rapid supply of synchronization clock signals that are necessary for timing regeneration.

The above replacement contains no new disclosure even though a portion is underlined. The underlined portion is merely moved to eliminate a blank line and has been in the original disclosure for the current application.